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Shaan (Aasmaan) Yadav

website:
shaan106.github.io

Education

Duke University — Expected May 2026
BSE:** Double major in **Electrical and Computer Engineering & Computer Science — *Durham, NC, USA*
***4.0 GPA** | Dean's List with Distinction*

Eton College — September 2017 – June 2022
***4.0 GPA** (all A* grades) | Oppidan (Academic) Scholar | House Captain | President of Scientific Society* — *Windsor, Berkshire, UK*

Relevant Courses & Skills

Courses – ECE 350 Digital Systems [A+], ECE 250 Computer Architecture [A+], ECE 280 Signals & Systems [A], ECE 552 Advanced Comp. Arch. I [Fall '24], ECE 230 Microelectronic Devices [Fall '24]

Languages – Python, Verilog, C/C++, Java, HTML/CSS, Matlab, Swift, Lua, Assembly

Technologies – Gem5, OpenSTA, CUDA, Skywater-PDK, Linux, Shell, FPGAs, PyTorch, Git, HPCs

Experience

Computer Architecture Researcher — August 2024 – present
Hilton Lab — *Duke University, NC, USA*

- Research under Prof Andrew Hilton on a novel leading-trailing checker chip architecture
- Simulations done using gem5, involving modifying existing components in C++ (ie X86 based OOO processors) and creating custom novel architectural extensions for TSV-based checker chip

Computer Architecture Researcher — May 2024 – Present
Yale Computer Systems Lab — *Yale University, CT, USA*

- Research under Prof. Bhattacharjee on Brain Computer Interface chips
- Leading research project for creating a modular globally-asynchronous-locally-synchronous hardware-level accelerator set simulator with built in optimization tools
- Custom creating python-RTL simulation, netlist latency and power estimation using openSTA and skywater 130nm processes
- Paper being submitted to conference November

Teaching Assistant — December 2023 – Present
Duke Electrical & Computer Engineering — *Duke University, NC, USA*

- Current TA for CS/ECE 350 (Digital Systems, Chip Design) under Prof. Bletsch, Prof. Board
- Previously TA for CS/ECE 250 (Computer Architecture) under Prof. Sorin and ECE 110 (Intro to ECE) under Prof. Daily
- Hold 6 hours of office hours for ~300 students every week, help create and grade quizzes & exams, assist with lectures

Raiz Vertical Farms — June 2023 – August 2023
Engineering Intern — *Lisbon, Portugal*

- Built computational models using self-collected data to show optimal combination of liquid flow rate, temperature and luminosity for maximising yield. Led to an annual yield increase of about 0.2 kg per square meter
- Transferred front-end app from obsolete technologies to Mantine v7; Connected environments to postgres SQL database; Refactored old React code into new environments

Relevant Projects

***more projects:** shaan106.github.io*

FPGA Boids — https://shaan106.github.io/projects.html#boids_fpga

- A highly efficient FPGA hardware level implementation of the boids algorithm. Custom Verilog hardware units, custom 5-stage pipelined CPU, custom compiler and display management system.

5-stage pipelined bypassed CPU — https://shaan106.github.io/projects.html#verilog_mips_cpu

- MIPS inspired ISA processor built from scratch using structural verilog. 32-bit 100MHz processor, Pipelined and Bypassed, Hazard handling, Wallace Tree multiplier, Restoring Division Divider, CLA adder

Other Experiences

Palantir *(Data Science Intern, '22)*, **Jaipur Foot** *(Field Volunteer, '21)*, **TeensInAI** *(ML Theory Teacher, '20-'21)*, **BBC** *(Intern, '19)*, Rock Climbing *(since '22)*, Fencing *(since '18)*