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Shaan (Aasmaan) Yadav

github & website:
github.com/shaan106
shaan106.github.io

Education

Duke University — Expected May 2026
BSE: *Double major in* ***Electrical and Computer Engineering & Computer Science*** — *Durham, NC, USA*
4.0 GPA | *Dean's List with Distinction*

Eton College — September 2017 – June 2022
4.0 GPA *(all A* grades)* | *Oppidan (Academic) Scholar* | *House Captain* | *President of Scientific Society* — *Windsor, Berkshire, UK*

Experience

GPU Intern — May 2025 – Present
Apple — *Austin, TX, USA*

- Working with the Apple GPU team during summer 2025, working with the power and performance team

Computer Architecture Researcher — August 2024 – Present
Hilton Lab — *Duke University, NC, USA*

- Research under Prof. Andrew Hilton on a novel leading-trailing checker chip architecture to enable aggressive microarchitecture designs without compromising chip accuracy or reliability
- Won the Duke ECE Department "Best Undergraduate Research" award for 2024
- Microarchitecture modelling done using gem5, extending OOO CPU components in C++ and creating novel components (ie custom cache hierarchies, validation schemes and instruction commit paths) for TSV-based checker chip

Teaching Assistant — December 2023 – Present
Duke Electrical & Computer Engineering — *Duke University, NC, USA*

- Teaching Assistant for CS/ECE 350: Digital Systems, previously for Computer Architecture and Fundamentals of ECE
- Guiding students in FPGA and gtkwave demos, providing breadboard and circuitry training, solving and analyzing boolean theory, and mentoring final FPGA-based projects
- Leading office hours sessions for ∼300 students every week, help create and grade quizzes & exams, assist with lectures

BCI Architecture Researcher — May 2024 – May 2025
Yale Computer Systems Lab — *Yale University, CT, USA*

- Research under Prof. Abhishek Bhattacharjee on Brain Computer Interface chips
- Full paper accepted into IEEE EMBC 2025 (first author)
- Led a research team to create a design tool that allows neurosurgeons to create hardware-level BCI accelerators
- Implemented a custom Python-based RTL simulation framework using OpenSTA to enable verification and evaluation of BCI hardware accelerators in a 130nm Skywater based process

Relevant Courses & Skills

Graduate Level Courses – Compilers [A], Advanced Comp. Arch. [A], Parallel Comp. Arch. [A], Fault Tolerant Sys. [A]
Undergrad Courses – Digital Systems [A+], Computer Architecture [A+], Signals & Systems [A], Microelectronic Devices [A]
Languages – Python, Verilog, C/C++, Java, HTML/CSS, Matlab, Swift, Lua, Assembly
Tools – Gem5, OpenSTA, CUDA, Skywater-PDK, Linux, Unix, TCL, Shell, Fusion, FPGAs, PyTorch, Git, HPCs

Relevant Projects

more projects: *shaan106.github.io*

FPGA Boids — https://shaan106.github.io/projects.html#boids_fpga

- A highly efficient FPGA implementation of the boids algorithm (modelling flocking behaviour in multi-agent environments)
- Designed and implemented parallel "BPU" computation units, and a custom C to assembly compiler, and a double-buffered VGA display wrapper to maximize refresh rate
- Full, in depth documentation: github.com/Shaan106/Boids_FPGA/

Other Experiences

Palantir *(Data Science Intern, '22)*, **Jaipur Foot** *(Field Volunteer, '21)*, **TeensInAI** *(ML Theory Teacher, '20-'21)*, **BBC** *(Intern, '19)*, Rock Climbing *(since '22)*, Fencing *(since '18)*